REMARKS

This paper is being provided in response to the Office Action dated October 5, 2005, for the above-referenced application. In this response, Applicants have amended claim 27 to clarify that which Applicants consider to be the invention. Applicants respectfully submit that the amendments to the claims are fully supported by the originally-filed specification.

Applicants gratefully acknowledge the allowance of claims 1-7 and 20-26.

The rejection of claim 27 under 35 U.S.C. 102(e) as being anticipated by U.S. Published Patent Application No. 2003/0189248 A1 to Estacio et al. (hereinafter "Estacio") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

Claim 27, as amended herein, recites a semiconductor device that includes an interconnect layer provided over a semiconductor substrate, an electrically conductive anti-oxidizing layer formed in contact with a part of the interconnect layer and containing a same element as an element in the interconnect layer that is chemically bonded or alloyed with a different element which is different from the element contained in the interconnect layer, and a bonding pad metal film provided over the electrically conductive anti-oxidizing layer to form an electrical conduction with the interconnect layer.

Estacio discloses increasing the number of MOSFET gate bump to make MOSFET gate contacts more durable and reliable. Extension of the under-bump metal laterally from the gate

contact with the gate pad metallization out to two or more gate pads overlying the source pad metallization reduces the risk of delamination of the metallization due to thermal and mechanical stresses in assembly and operation. Estacio discloses an interconnect layer (51) provided over a semiconductor substrate (7), an anti-oxidizing layer (52), and a metal film (53) formed on the anti-oxidizing layer (52).

Applicants' independent claim 27, as amended herein, recites a semiconductor device having an interconnect layer and an anti-oxidizing layer, containing a same element as in the interconnect layer and a different element than is in the interconnect layer, disposed between the interconnect layer and a bonding pad metal film. The oxidation of the interconnect metal is effectively inhibited by the action and configuration of the anti-oxidizing layer, even when a part of the interconnect layer is exposed by the contact of the probe. Since the semiconductor device as presently claimed has the anti-oxidizing layer between the interconnect layer and the protective film, even though the upper layer of the interconnect layer is damaged in the case of being poked with the probe and the surface of the interconnect layer is exposed, the different element in the anti-oxidizing layer, which is different from an element contained in the interconnect layer, is oxidized by containing the atmospheric air. Thus, the chemically stable layer that, for example, prevents the corrosion of copper is formed on the surface of the interconnect layer, and thereby inhibiting the deterioration of the semiconductor device.

The present claimed invention prevents the corrosion of the interconnect layer in the case of being poked with the probe, by providing the synergistic effect of the protective film and the anti-oxidizing layer configured as claimed. (See page 6, lines 9 - page 7, line 4 of the present

application.) In particular, the anti-oxidizing layer configured as recited and including a same element as is in the interconnect layer that is chemically bonded or alloyed with a different element from the interconnect layer more surely inhibits the undesired corrosion. (See page 10, lines 4-11 and page 13, lines 10-24 of the present application.)

Applicants respectfully submit that Estacio does not teach or fairly suggest at least the above-noted features as claimed by Applicants. Accordingly, Applicants respectfully request that this rejection be reconsidered and withdrawn.

The rejection of claims 28-31 under 35 U.S.C. 103(a) as being unpatentable over Estacio in view of U.S. Published Patent Application No. 2003/0052414 A1 to Cowens et al. (hereinafter "Cowens") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

Claims 28-31 depend from claim 27, discussed above.

Estacio is discussed above.

The Cowens reference discloses a plasma condition method for improving adhesion between an integrated circuit chip and an insulating underfill material.

Applicants respectfully submit that Cowens reference does not overcome the above-noted deficiencies of the Estacio reference with respect to Applicants' claim 27, from which claims 28-

31 depend. Accordingly, Applicants respectfully request that this rejection be reconsidered and withdrawn.

Based on the above, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 508-898-8603.

Respectfully submitted,
MUIRHEAD AND SATURNELLI, LLC

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Donald W. Muirhead
Registration No. 33,978

Customer No.: 26339

Muirhead and Saturnelli, LLC
200 Friberg Parkway, Suite 1001
Westborough, MA 01581
Phone: (508) 898-8601
Fax: (508) 898-8602